REMARKS

The claims are claims 1 to 7 and 9 to 12.

Claims 1 to 7, 9 and 12 were rejected under 35 U.S.C. 102(b) as anticipated by Swanstrom U.S. Patent No. 5,754,884. The OFFICE ACTION states that the claimed source increment size register is anticipated by increment source address register 808 and the destination increment size register is anticipated by increment destination register 810 illustrated in Figure 8 of Swanstrom.

Claim 1 recites subject matter not anticipated by Swanstrom. Claim 1 recites "a source increment size register storing a source increment size," "recalling data from a first bus data supplying device beginning at said source start address and thereafter at successive addresses differing by said source increment size," a target increment size register storing a target increment size" and "supplying said recalled data to a first bus data receiving device beginning at said target start address and thereafter at successive addresses differing by said target increment size." These portions of claim 1 require the address interval between successive source data to be set by the source increment size register and the address interval between successive destination data to be set by the target increment size register. The increment source address register 808 and the increment destination source address register 810 fail to anticipate these limitations. Swanstrom states at column 9, lines 32 to 42:

> "In the case where the source or destination address is system memory, DMA controller 750 increments the address which it supplies on expansion bus 730 by the word size after each word transfer. However, typically in the case where the source or destination is a peripheral device the address is fixed, commonly at a fixed I/O cycle address, hence DMA controller 750 does not increment the address which it supplies on expansion bus 730 after each word transfer. CPU 710 programs increment source address register 808 and increment

> destination address register 810 to indicate whether or not to increment the respective expansion bus address after a word transfer."

Swanstrom further states at column 9, lines 54 to 58:

> "For example, increment source address register 808 and increment destination address register 810 may be implemented as each single bits within a common latch or SRAM location."

This disclosure of Swanstrom clearly indicates incrementing by the word size, which Swanstrom discloses is set by the cycle-type register 870. The increment source address register 808 and increment destination address register 810 only indicate whether or not to increment the address. The disclosure at column 9, lines 54 to 58 teaches a single bit for this purpose. Such a single bit is sufficient to indicate whether to increment or not increment. A single bit is not sufficient to indicate the amount of the increment as recited in claim 1. Note claim 1 recites differing structures to store word size and increment amount while Swanstrom teaches only a single structure cycle-type register 870 for controlling both these features. This application teaches at page 5, liens 13 to 14 "The address increment size is not dependent upon the word size of the transfer." Accordingly, claim 1 is not anticipated by Swanstrom.

Claims 2 to 7 and 9 to 12 are allowable by dependence upon allowable claim 1.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

Robert D. Marshall, Jr.
Reg. No. 28,527